



TECHNOLOGY CENTER 2000

The following three U.S. Patents reveal processes for dual gates and dummy gates:

- 1) U.S. Patent 6,159,782 to Xiang et al., "Fabrication of Field Effect Transistors Having Dual Gates with Gate Dielectrics of High Dielectric Constant."
- 2) U.S. Patent 5,960,270 to Misra et al., "Method for Forming an MOS Transistor Having a Metallic Gate Electrode that is Formed After the Formation of Self-Aligned Source and Drain Regions."
- 3) U.S. Patent 6,043,157 to Gardner et al., "Semiconductor Device Having Dual Gate Electrode Material and Process of Fabrication Thereof."

Sincerely,

A handwritten signature in black ink, appearing to read 'SBA', with a stylized flourish at the end.

Stephen B. Ackerman,
Reg. No. 37761

Form PTO-1449

INFORMATION DISCLOSURE CITATION
IN AN APPLICATION

(Use several sheets if necessary)

Document Number (Optional)

TSMC-6-133

Application Number

09/905,408

Applicant

Sheng-Hsiung Chen et al.

Filing Date

07/16/01

Group Art Unit

2812

U. S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	TITLE	CLASS	SUBCLASS	FILED DATE & APPROPRIATE
	6 0 8 7 2 3 1	7/11/00	Xiang et al.	438	287	8/5/99
	6 1 5 9 7 8 2	12/12/00	Xiang et al.	438	197	8/5/99
	5 9 6 0 2 7 0	9/28/99	Misra et al.	438	197	8/11/97
	6 0 4 3 1 5 7	3/28/00	Gardner et al.	438	692	12/18/97

FOREIGN PATENT DOCUMENTS

DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
					YES	NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER

DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP §609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.


 RECEIVED
 OCT-4 2001
 TELECOMMUNICATIONS